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Controlled Single-Cooper-Pair Charging Effects in a Small Josephson Junction Array

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We report on measurements of single-Cooper-pair charging effects in small Josephson junction arrays, and the experimental techniques that were used. We succeeded in having complete control over the array's electrostatic parameters; offset charges were accurately compensated, and the poisoning of 2*e*-periodic effects by quasiparticles was circumvented. This allowed for a controlled study of the array's coherent ground state. A few measurements gave results which were not fully 2*e*-periodic due to interesting parity effects. The arrays are in the regime where the energy scales for the Josephson effect and single-charge effects are comparable.

KEY WORDS: Josephson effect; single-charge effects; parity effects.

Josephson junction arrays consist of small superconducting islands that are connected by tunnel junctions. In arrays of junctions with a very small capacitance *C,* single-charge effects play an important role [1]; fluctuations in the number of excess Cooper pairs on the islands are suppressed by the Coulomb charging energy of the islands. In the regime where the energy scale for the single-charge effects $E_C = e^2/2C$ is comparable to the Josephson energy E_J of the junctions, several macroscopic quantum phenomena have been observed [2–6]. These are a consequence of the conjugation relations between the array's macroscopic charge and phase variables.

In the regime with $E_J \approx E_C$, a quantum mechanical description of the array is needed. The macroscopic ground state can be described as a coherent superposition of charge configurations with a well-defined number of excess Cooper pairs on each island [3,7]. In systems with only a few islands, the electrostatic energy of each of the charge configurations can be controlled by means of gate electrodes that are capacitively connected to the islands. It is then possible to control the form of the ground state. In superconducting double-junction circuits, a 2*e*-periodic modulation of the maximum supercurrent that can flow through the circuit has been observed [3,4]. Van Oudenaarden has observed a 2*e*-periodic superconductor to Mott-insulator transition in a linear array with six islands [6].

In practice, two phenomena hamper a controlled study of the coherent superposition of charge configurations. One is the presence of background charges; each island is polarized by a random offset charge, caused by, e.g., impurities in the underlying substrate. Also, parity effects can be a problem; the presence of quasiparticles in the circuit suppresses the formation of a coherent ground state [3,8]. The offset charges must be compensated by gate-induced charges, and the presence of quasiparticles needs to be circumvented.

In this article we present experimental results from measuring single-charge effects in small Josephson junction arrays, with complete control over the electrostatic parameters. Results were 2*e*-periodic in the induced gate charges (Fig. 1a). Along with results we report on the experimental techniques that were used. The array was designed for studying charge-fluxoid duality [7]. Experimental results in light of these phenomena will be presented in a parallel article [9]. The arrays consist of two small superconducting islands connected to each other and to macro-

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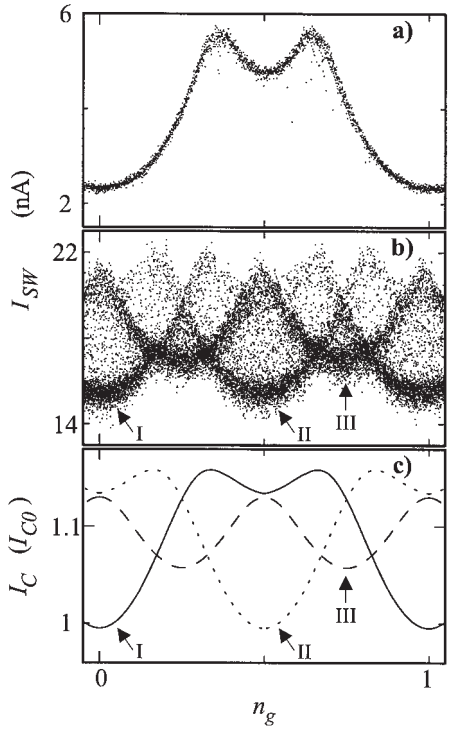

Fig. 1. The switching current I_{SW} as a function of charge frustration. (a) Results of 2,000 individual switch events measured while slowly sweeping the induced charge $n_g = C_g V_g/2e$ on both gates simultaneously (array 3, $\Phi = 0$, $T = 70$ mK). (b) Results of 20,000 individual switch events. Three levels appear due to parity effects, i.e., quasiparticles in the array (array 1, $\Phi = 0$, $T = 10$ mK). (c) Numerical simulations of the array's critical current I_C versus n_g [I_C in units of $I_{C0} = (2e/\hbar)E_J$], based on [7], with $E_J/E_C = 0.5$. Trace I is for the (even–even) parity configuration, II is for (odd–odd), III is for (odd–even) and (even–odd).

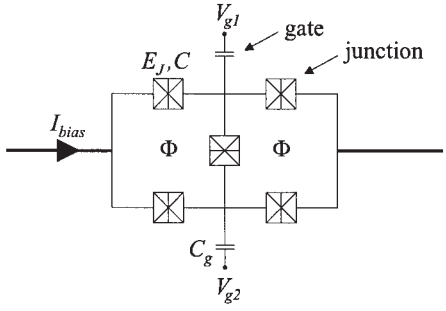

Fig. 2. Schematic of the Josephson junction array. Two small superconducting electrodes are coupled to each other and to leads by small tunnel junctions. The junctions have equal Josephson coupling E_J and capacitance C. The voltage V_g on capacitively connected gates controls the gate-induced charge. The bias current I_{bias} is injected via macroscopic leads. A magnetic flux Φ can be applied to the loops.

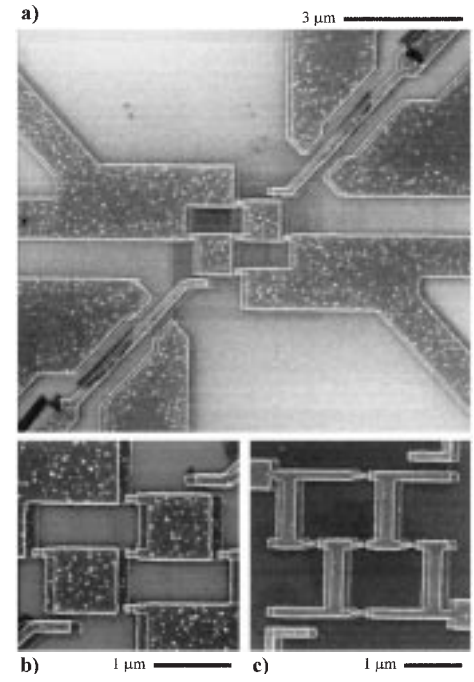

Fig. 3. SEM-graphs of the array. In (a) the two islands are in the center. From the top-left and bottom-right, leads are connected in a four-point setup. Two gate electrodes approach the array from the top right and bottom left, surrounded by grounded gate electrodes. The graphs below illustrate the difference in island shape between arrays 2 and 3 (b) and between arrays 1, 4, 5 and (c).

scopic leads by small Josephson junctions with $E_J \lesssim E_C$ (Figs. 2 and 3). The voltage V_g on capacitively connected gates controls the gate-induced charge $n_g = C_g V_g/2e$ (this definition assumes that offset charges have been compensated already). Another control parameter for the array is the magnetic flux Φ threading the loops, but in this article we will focus on charging effects and limit ourselves to the case with $\Phi = 0$. We performed measurements on five different arrays (Table 1). The arrays were studied by measuring the maximum supercurrent that can flow through the array, called the switching current.

The arrays with $Al–Al_2O_3–Al$ junctions of about $(100\ nm)^2$ were fabricated with standard *e*-beam lithography in a double-layer resist and shadow evaporation techniques [10,11]. Two successive aluminum layers were deposited (35 and 55 nm) on thermally oxidized Si substrates by *e*-beam evaporation. We used aluminum of 0.9999 purity or higher, and evaporated in a vacuum below 10^{-7} mbar (below 10^{-6} mbar during evaporation). The tunnel barriers were formed by exposing the first aluminum layer at room temperature to ~0.1 mbar of pure O_2 for 5 min. The

Table I. Properties of Arrays 1–5[a]

Array	E_J (μeV)	E_C (μeV)	E_J/E_C	Δ (μeV)	C_g (aF)	*CRC* shunt	Filters and shielding	*e*/2*e*
1	71	1.5×10^2	0.5	198	33	no	I & II	*e*/2*e*
2	31	1.4×10^2	0.2	208	40	yes	II	2*e*
3	30	1.5×10^2	0.2	209	40	yes	II	2*e*
4	16	1.8×10^2	0.1	223	80	no	II	—
5	15	1.9×10^2	0.1	220	80	no	II	—

[a] E_J was estimated from experimentally determined values of the tunnel resistance R and the gap Δ, using $E_J = h\Delta/8e^2R$. R and E_C were estimated from the differential resistance and the voltage offset in the high-bias *IV* [19]. Δ was directly measured in the low-bias *IV*. C_g was estimated from Coulomb oscillations in the normal state (applying a 1-T magnetic field) to avoid ambiguity about *e* or 2*e* periodicity. The last columns indicate the presence of an on-chip *CRC* shunt-network, what copper powder filter and shielding set was used, and whether results were *e* or 2*e* periodic. Filter set II proved effective for obtaining 2*e* periodicity from these measurements. Set I proved effective in the measurements of [4].

on-chip leads and pads for bonding were also made of aluminum and deposited in this evaporation step. On arrays 2 and 3 we successively fabricated with a second lithography and evaporation step (60 nm SiO, 5 nm Ti, 25 nm Au) an on-chip *CRC*-network that was shunting the array. The layout was such that there was in the direct vicinity of the array an overlap of $(140\ \mu\text{m})^2$ with the array's bias leads on both sides. These two gold pads were connected by a 200-μm-long, 0.3-μm-wide gold line, which had a resistance of 3 kΩ at milliKelvin temperatures. The parallel plate capacitors had each a capacitance of about 10 pF [11]. This shunt network dissipates voltage oscillations created by the array at frequencies above $\sim$0.1 GHz, and is crucial for a clear observation of the zero-voltage supercurrent branch at low effective Josephson coupling [3]. With arrays 4 and 5, which did not have an on-chip *CRC*-environment, premature switching from the zero-voltage state occurred below 10 pA. These results were too noisy for observing charging effects.

The gates were surrounded by a grounded guard structure (Fig. 3a) to reduce the cross-capacitance between a gate electrode and the island on the other side of the array. With grounded guards the cross-capacitance was about $0.1C_g$. In a measurement where the guard was not grounded, but at the same potential as the gate electrode, the cross-capacitance was higher by a factor of 3.

Measurements on the arrays were performed in a dilution refrigerator with a base temperature below 10 mK. The samples were mounted on the cold finger in a microwave-tight copper box, surrounded by a sequence of low-temperature shields. All wires to the samples were filtered by copper powder filters at base temperature, and rfi-feedthrough filters at room temperature. The switching current was measured in a four-point setup. It was probed by dedicated low-noise electronics which ramps a bias current through the array, and records the value of the current at which the system switches from the zero-voltage supercurrent branch to a finite voltage. After switching the current is reduced to zero. A typical value for the ramp rate of the current was 10 nA/ms, at a repetition rate of 20 Hz. The voltage probes for the four-point wiring were connected on chip in the direct vicinity of the array (Fig. 3a). Voltages were amplified 20,000 times by a battery-powered preamplifier in series with the dedicated electronics. With a noise floor of 0.4 μV RMS, the reference voltage for switching was set to 2 μV. The gates were connected via 1:100 voltage dividers at the mixing chamber (total resistance 1 MΩ, with a 150-Hz low-pass *RC* filter). Additional optically decoupled 1 : 1 isolation amplifiers and 1-Hz low-pass *RC* filters at room temperature improved the results of switching current measurements significantly (higher level, less scatter, and less parity effects).

Figure 1a shows a single period of the 2*e*-periodic modulation of the switching current that we observed in arrays 2 and 3. The observed modulation is in very close agreement with results of numerical simulations (as level I in Fig. 1c, but with E_J/E_C as estimated for array 3), based on a quantum description of the array in the charge basis [7]. The presence of quasiparticles was successfully circumvented and, as will be discussed below, offset charges were compensated to within 0.01 of a 2*e* gate charge. Offset charges remained stable on a time scale of hours. This allowed for a study of the switching current while sweeping through the entire V_{g1}–V_{g2} plane, and peak positions measured on arrays 2 and 3 demonstrated a clear honeycomb structure with a fundamental period of 2*e*. Results from array 1, however (Fig. 1b), suffer

from parity effects. We observed three distinct levels in the swithcing current as a function of gate charge, which we can relate to the presence of quasiparticles in the array. The array has two islands that can each have an even or odd charge state, giving four different parity configurations for the entire array. As illustrated in Fig. 1c, the presence of a quasiparticle on one of the islands is effectively the same as applying a gate charge of e. Level I (even–even) in Fig. 1b and 1c is equal to level II (odd–odd) shifted over a distance e. Level III is for the parity configurations (even–odd) and (odd–even). This interpretation was confirmed by measurements where both gates were swept simultaneously, but with a constant offset between n_{g1} and n_{g2}. Level III then split up into two different levels, again in very close agreement with simulations. The Saclay group observed very similar quasiparticle phenomena in an array with the same layout [12]. For each individual measurement of the switching current, the probability of finding the array in one of the four parity configurations was approximately equal. This indicates an interesting interplay between the measurement time scales and the time scales at which the parity of the array changes. It was indeed observed that the probability for measuring high levels of the switching current decreased with decreasing ramp rate of the bias current [12,13].

Figure 4 illustrates how some parity effects remained present in arrays 2 and 3. Mostly around gate charges corresponding to $n_g = \frac{1}{2}$, the switching current was sometimes jumping between two distinct levels. The jumps were often to a value that corresponds to the level of the switching current at exactly e shifted in gate charge (Fig. 4c). Moreover, measurements in the normal state (superconductivity suppressed with a 1-T magnetic field) showed that the background charges were very quiet on the time scale of the jumps. This proves that jumps are due to parity effects, and not to random changes of offset charges in the background. An important difference with the parity effects of Fig. 1b is that the parity of the islands remains unchanged over many sequential switch events (Figs. 4b and 4c). Note that for each individual point in the traces of Figs. 1 and 4, the voltage over the array switched to the superconducting gap $2\Delta/e$. After each switch event, many quasiparticles are thus created in the array for a short time, but the parity configuration is usually not affected. This indicates that the parity effects involve tunneling of conduction electrons to localized states on the islands. This model for parity effects was proposed by Eiles *et al.* after observing infrequent jumps of exactly e in the gate-

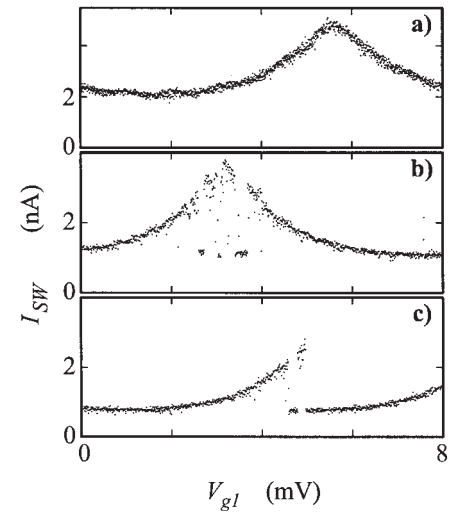

Fig. 4. The switching current I_{SW} versus V_{g1}, with gate 2 at $n_{g2} \approx 0$. The V_{g1} voltage window corresponds to a gate charge of $2e$. In (a), $2e$ periodicity is not disturbed by quasiparticles (array 3, $\Phi = 0$, $T = 70$ mK). In (b) and (c), $2e$ periodicity is disturbed by a quasiparticle jumping onto island 1, which results in two distinct levels in I_{SW} (array 2, $\Phi = 0\ \Phi_0$, $T = 30$ mK). (c) illustrates that the additional level in I_{SW} is equal to the undisturbed level shifted over a distance e (4 mV).

charge dependence of a normal superconductor–normal double junction circuit [14].

The parity effects presented in Figs. 1b and 4 had a very weak temperature dependence up to $T \approx 150$ mK. In array 3, e.g., the presence of quasiparticles in the array decreased when raising the temperature from 10 to 70 mK. Raising the temperature further, the parity effects changed drastically at $T^* \approx 150$ mK, in agreement with the odd–even free-energy model of Tuominen *et al.* [15,16]. Here poisoning by thermally excited quasiparticles becomes dominant. The switching current turned e-periodic, and had much lower values. Also, the switching results had large scatter, instead of one or more distinct levels. To avoid quasiparticles in the system it is crucial to have the charging energy of the islands ($\sim E_C/3$) lower than the odd–even free-energy difference D [15,16]. At milliKelvin temperatures and for aluminum islands with dimensions as in Fig. 3, $D \approx \Delta$. Even though this requirement was satisfied in all the arrays (Table 1), the results of array 1 were strongly influenced by the parity effects, and also in arrays 2 and 3 some of the parity effects were observed. The argument that the occupation of odd charge states is very unlikely for $E_C/3 < \Delta$ assumes that the small superconduting islands have a perfect BCS gap. For small

islands, however, it is hard to predict what the influence is of boundaries and impurities on the formation of the BCS gap [17]. The islands in Fig. 3c have a thickness and width not much larger than the grain size of the evaporated aluminum. Also, due to the shadow evaporation technique, the island consists in fact of two islands on top of each other, connected by a very large tunnel junction [18]. In practice this may lead to quasiparticle states within the gap. For this reason, we changed the design of the islands for arrays 2 and 3 after the measurements on array 1.

The design of the island was changed from the branched structure of Fig. 3c (also the island shape of the device in [12], with parity effects) to the lumped shaped of Fig. 3b (also the island shape of the six-island arrays of [6], with little parity effects). This was done at the cost of a lower odd–even free-energy difference D due to the larger island volume. We found that in arrays 2 and 3 the quasiparticle presence was almost fully suppressed. This is an indication that the shape of mesoscopic islands plays a role in avoiding poisoning by quasiparticles. However, we cannot rule out that the on-chip CRC-environment in arrays 2 and 3 has influenced the relaxation rates for quasiparticles. We also cannot rule out that uncontrolled microscopic differences in the materials, e.g., impurities, have played a crucial role (array 1 was evaporated in a different setup than the other arrays).

We developed a computer-controlled method which accurately compensates the offset charges, usually in a few minutes. We calibrated our gate charges by searching for gate values that give a minimum switching current for both gates simultaneously. This corresponds to finding the minimum in the honeycomb peak structure in a V_{g1}–V_{g2} plane of $2e$ by $2e$. This was done in an iterative manner since the islands are capacitively coupled, and because of the presence of the small cross-capacitance. The gate capacitance of each island was determined accurately, such that we could sequentially sweep the voltage on one of the gates over a window corresponding to exactly $2e$. After the sweep the gate was left at the value for which the minimum in the switching current was found. When one gate was at $n_g \approx 0$, the modulation of the switching current by the other gate was as in Fig. 4a. We determined the minimum by searching for the maximum in the cross-correlation $\sigma[j]$ between the data and a phenomenological peak shape $\exp(-3.5|i - N/2|/N)$, where

$$\sigma[j] = \sum_{i=1}^{N} I_{SW}(V_g[i] - V_{\text{off}}[j]) \exp(-3.5|i - N/2|/N)$$

Here N is the number of measured switch events while sweeping over the $2e$ period, and i is an index for the sequence of measured I_{SW} at gate voltage $V_g[i]$. The index j is the running-shift variable for the cross-correlation. The data set I_{SW} is shifted modulo the $2e$ gate-voltage window. We used N = 1,000. The advantage of this method is that is makes optimal use of all N measurements of a stochastic variable. Also, the method is very robust against a moderate presence of parity effects, as in Fig. 4b. We considered the offset charges successfully tuned away when the same offset voltages were found in five successive iteration steps. The criterion here was that the standard deviation of the five results was less then 0.01 of a $2e$ period. This accuracy was confirmed by independent observations from sweeping the gates over very long intervals.

In summary, we succeeded in measuring $2e$-periodic single-charge effects in a small Josephson junction array. The presence of quasiparticles in the array was successfully suppressed in a few of the arrays. Our results indicate that processes on a long time scale, in which conduction electrons can be trapped in localized states in the islands, play an important role in the origin of parity effects in small superconducting islands. We developed a computer-controlled method which accurately compensates offset charges in the array.

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